DETAILED ACTION

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oikawa 6,316,998 B1 or Ogawa et al. 04-154342 taken with Hieda (2002/0011612), Aller et al. 6,909,147 B2, Fitzerald 2003/0057439 A1, and optionally Sugawa et al. (EP 1347506).

Re claims 1-6, Oikawa teaches a DC amplifier comprising a differential amplifier circuit including a MISFET transistor MP1 and MISFET transistor MP2. See Fig. 1, column 5 lines 4-36. Ogawa et al. also teach DC amplifier comprising differential circuit 1 employing MISFET transistor Tr1-Tr5 as shown in Fig. 4 and the abstract. Thus either Oikawa or Ogawa et al. lack primarily the showing of the MISFET having components as characterized and the recitation of the gate heights of the p channel and n channel MIS being different and the current drive capabilities of the N-channel and of the P-channel MIS can be substantially equal.

Hieda teaches MISFET transistor in which projection portion 13 is formed by a silicon substrate 10 having a first crystal surface as a primary surface and a second crystal surface as a side surface, a gate insulating film 18 on at least a part of a top surface and the side surface of the projecting portion 13, a gate 16 on the gate insulating film and source/drain 17 on both sides enclosing the gate insulating film. The various advantages include larger channel width, smaller planar surface area, improved carrier mobility, prevention of punch-through. The use of both n channel or p channel, e.g., as claimed in claim 6, is also shown, e.g., [0418], Figs. 48D, [0427] wherein CMOS circuit can be made including various ways to form nFET and pFET of different channel

widths. See Figs. 1-4, 12, 20, 33, 48, and the corresponding descriptions, particularly [0175]-[0182], [0417]-[0435], [0501]-[0541].

Aller et al. 6,909,147 B2 teaches FinFET devices having first and second fins of different heights. By increasing the fin height or decreasing the fin heights, the channel width can be varied accordingly. The ratio of the height of the first fin to the height of the second fin can be used to allow to alter the channel width of the FETs within the devices thereby tuning the performance of the transistors to the designer performance. See the abstract, Figs. 7-10, column 2 line 18 to column 6 line 22.

It would have been obvious to one skilled in the art in practicing Oikawa or Ogawa et al. to have employed the MIS transistors in the above circuit since such devices have improved characteristics as taught by Hieda. The selection of the different heights for the nFET and pFET would have been conventional and obvious as evidenced by Aller et al. where such would permit selection of the desired channel widths in the respective transistors. Regarding the hydrogen removal from silicon surface using plasma, such correspond to a product by process limitation that does not impart patentability to the claims. It is well settled that a "product-by-process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al., 227 USPQ 964 (CAFC, 1985)* and the related case cited therein which make it clear that it is the final product per se which must be determined in a "product-by-process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product-by-process" claims or not. As stated in *Thorpe,*

Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA, 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147(CCPA 1969).*

When the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claimed in a product-by-process claim, a rejection based alternatively on either section 102 or section 103 of the statute is eminently fair and acceptable. As a practical matter, the Patent Office is not equipped to manufacture products by the myriad of processes put before it and then obtain prior art products and make physical comparisons therewith." In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972).

"The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. In re Fessmann, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983)

Alternatively, such hydrogen removal in plasma would have been conventional and obvious as evidenced by Sugawa et al. the abstract [0015]-[0023] to improve device characteristics including leakage current and break down current.

Regarding the amended recitation of the gate heights being different so that the current drive of the N channel and P channel device can be substantially the same would have been conventional and obvious as delineated in Aller et al. above and in view of Fitzgerald 2003/0057439 A1, [0006]-[0011] which evidences that the NMOS and PMOS transistors can be designed to provide approximately equal driving capability by appropriately adjusting the widths of the gates, thereby permitting the balance of the

respective current drives whereby device performance can be improved, e.g., [0011], including by widening the PMOS transistor, i.e., the width of the gate of the PMOS, [0008], to minimize stage delay. Note that in the case of FETs employing fins (or projections in applicant's terminology), the effective channel width is proportional to the fin heights (column 3 lines 53-64).

Re claim 2, the channel width being a total width of top surface and of the side surface is apparent in the figures above given the positioning of the gate by nature of the fins employed as discussed above. Re claim 3, the respective surfaces are shown in the figures in Hieda, including recitation of (100), ,e.g., [0175], [0181]; and the (110) surface as the side surface would have been apparent or obvious given their orientation as shown in the figures.

Re claims 4 and 5, the use of a third MIS MP3 to connect to source or drain of the first and second MIS MP1, MP2, as well as a fifth and sixth transistors is also shown in Fig. 1 of above in Oikawa and Fig. 4 of Ogawa wherein the respective constant current source and circuit would result. A recitation directed to the manner in which a claimed apparatus is intended to be used does not distinguish the claimed apparatus from the prior art – if the prior art has the capability to so perform. See MPEP 2114 and *Ex parte Masham,* 2 USPQ2d 1647 (1987). The recitation of a new intended use for an old product does not make a claim to that old product patentable. *In re Schreiber*, 44 USPQ2d 1429 (Fed. Cir. 1997).

Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:00 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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/Tuan N. Quach/
Primary Examiner, Art Unit 2826